Claims

What is claimed is:

1. A memory system comprising:

a memory controller; and

a plurality of memory banks operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, wherein a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks;

the memory controller being adapted to process requests for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests.

2. The memory system of claim 1 wherein the minimum number of the memory banks for storage of the multiple copies of the given data item is determined as a function of a random cycle time of the memory banks.

3. The memory system of claim 2 wherein the minimum number of the memory banks for storage of the multiple copies of the given data item is determined as a function of the random cycle time of the memory banks and a random bank access delay of the memory banks.

4. The memory system of claim 3 wherein the minimum number of the memory banks for storage of the multiple copies of the given data item is determined as an integer greater than or equal to a ratio of the random cycle time of the memory banks to the random bank access delay of the memory banks.

5. The memory system of claim 1 wherein each of at least a subset of the plurality of memory banks is configured to store the same plurality of data items, the subset comprising at least two of the memory banks.

6. The memory system of claim 1 further comprising a first memory channel including the plurality of memory banks as a first plurality of memory banks and a second memory channel including a second plurality of memory banks.

7. The memory system of claim 6 wherein the memory controller further comprises a first controller coupled to each of the first plurality of memory banks via a first set of address, data and control buses, and a second controller coupled to each of the second plurality of memory banks via a second set of address, data and control buses.

8. The memory system of claim 1 wherein the memory controller further comprises:

a set of queues configured for storing the access requests, each of the queues being associated with a corresponding one of the plurality of memory banks; and

an arbiter operatively coupled to the set of queues for selecting a given one of the access requests therefrom in accordance with the specified bank access sequence.

9. The memory system of claim 8 wherein the specified bank access sequence comprises a round-robin selection sequence in which particular ones of the access requests are selected in a round-robin sequence from head positions of the sets of queues and applied to corresponding ones of the plurality of memory banks.

10. The memory system of claim 1 wherein each of at least a subset of the plurality of memory banks is implemented using one or more dynamic random access memory (DRAM) devices.

11. The memory system of claim 10 wherein one or more of the DRAM devices comprises a fast cycle DRAM (FCDRAM) device.

12. The memory system of claim 1 being operable in multiple modes, the multiple modes comprising at least:

a first mode in which a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks, and the memory controller is adapted to process requests for access to the data items stored in the memory banks in accordance with the specified bank access sequence; and

a second mode in which the given data item is stored as a single copy of the data item with the single copy in a particular one of the plurality of memory banks, and the memory controller is adapted to process requests for access to the data items stored in the memory banks in accordance with a sequence other than the specified bank access sequence.

13. The memory system of claim 1 wherein the access requests comprise a plurality of read requests.

14. The memory system of claim 1 wherein the system processes the access requests in the form of a plurality of read requests and a plurality of write requests, the read requests and the write requests being in an unbalanced ratio favoring the read requests.

15. A processing system comprising:

a processing device; and

a memory system operatively coupled to the processing device, the memory system comprising:

a memory controller; and

a plurality of memory banks operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, wherein a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks;

the memory controller being adapted to process requests received from the processing device for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests.

16. The processing system of claim 15 wherein the processing device comprises a network processor.

17. The processing system of claim 16 wherein the memory system implements an external tree memory for the network processor.

18. A method for use in a memory system comprising a memory controller and a plurality of memory banks operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, the method comprising:

storing a given data item as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks; and

processing in the memory controller requests for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests.

19. A method for use in a memory system comprising a memory controller and a plurality of memory banks operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, the method comprising:

determining a minimum number of the memory banks for storage of multiple copies of a given data item as a function of a random cycle time of the memory banks; and

storing the given data item as multiple copies of the data item with a given one of the multiple copies in each of the designated minimum number of the memory banks.